Cover Page

EE 316-08

Electric Circuits & Electronics Design Lab

**Lab 7 & 8: Characteristics of BJT and Amplification Behavior**

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**Lab Date: 03/22/2021**

**Lab Due: 03/25/2021**

**1. Introduction:**

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| This lab introduces and expands the ideas and theory behind bipolar junction transistors (BJTs). We will first cover the theory behind BJTs in section 2 and then simulate them using Multisim in section 3. Afterwards, I will discuss the results and wrap the lab up with a short conclusion in section 6. Lastly, I will perform some simple hand calculations and they can be seen in the appendix. |

**2. Theoretical Analysis:**

**2.1 Construction (NPN)**

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| A typical BJT has a collector, base, and emitter region. NPN bases’ have P=type materials (ones with more holes) and emitters that are N-type that have more electrons. The emitter region of an NPN contains a higher density of electrons than the collector which allows current to flow from the collector to the emitter. A NPN can be seen in figure 1.    Figure 1: Basic NPN |

**2.2 Construction (PNP)**

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| A typical BJT has a collector, base, and emitter region. PNP bases’ have N-type materials and emitters that are P-type. The emitter region of an PNP contains a higher density of holes than the collector which allows current to flow from the emitter to the collector. A PNP can be seen in figure 2.    Figure 2: Basic PNP |

**2.3 Operation**

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| Current flows through the base region if the transistor is in “forward” or “reverse-active mode”. Forward means the DC current is flowing in the direction of the base-collector junction and in the opposite direction of the base-emitter junction. Reverse is just the opposite. Saturation mode is when max current flow is achieved, and no current flowing is cut-off mode. Figure 3 shows this visually.    **Figure 3: Output characteristics of a BJT** |

**2.4 Appearance**

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**3. Simulations:**

**3.1 Common collector circuit (Lab 7)**

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| Circuit 1 shows the common collector circuit in multisim. I will then show the relationship between VCE and IC in table 1 and graph 1. Section 5 will comment on the results.    Circuit 1: Common collector circuit in multisim.   |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | V1 (V) | V2 (V) | IB (mA) | IC (mA) | IE (mA) | VCE (V) | β | | 4 | 0 | 0.012 | -0.01 | 0.00 | -0.01 | -0.661 | | 4 | 0.5 | 0.011 | 0.379 | 0.39 | 0.379 | 34.455 | | 4 | 1 | 0.011 | 0.701 | 0.712 | 0.701 | 63.727 | | 4 | 1.5 | 0.011 | 0.707 | 0.718 | 0.706 | 64.273 | | 4 | 2 | 0.011 | 0.711 | 0.722 | 0.711 | 64.636 | | 4 | 2.5 | 0.011 | 0.716 | 0.727 | 0.716 | 65.091 | | 4 | 3 | 0.011 | 0.721 | 0.732 | 0.721 | 65.545 | | 4 | 3.5 | 0.011 | 0.725 | 0.736 | 0.725 | 65.909 | | 4 | 4 | 0.011 | 0.73 | 0.741 | 0.73 | 66.364 | | 6 | 0 | 0.018 | -0.011 | 0.01 | -0.011 | -0.611 | | 6 | 0.5 | 0.018 | 0.399 | 0.417 | 0.399 | 22.167 | | 6 | 1 | 0.018 | 0.857 | 0.874 | 0.856 | 47.611 | | 6 | 1.5 | 0.017 | 1.195 | 1.212 | 1.194 | 70.294 | | 6 | 2 | 0.017 | 1.203 | 1.221 | 1.203 | 70.765 | | 6 | 2.5 | 0.017 | 1.211 | 1.229 | 1.211 | 71.235 | | 6 | 3 | 0.017 | 1.219 | 1.237 | 1.219 | 71.706 | | 6 | 3.5 | 0.017 | 1.227 | 1.245 | 1.227 | 72.176 | | 6 | 4 | 0.017 | 1.235 | 1.253 | 1.235 | 72.647 | | 8 | 0 | 0.025 | -0.012 | 0.012 | -0.012 | -0.480 | | 8 | 0.5 | 0.025 | 0.41 | 0.434 | 0.41 | 16.400 | | 8 | 1 | 0.025 | 0.878 | 0.903 | 0.878 | 35.120 | | 8 | 1.5 | 0.024 | 1.345 | 1.369 | 1.345 | 56.042 | | 8 | 2 | 0.024 | 1.709 | 1.733 | 1.708 | 71.208 | | 8 | 2.5 | 0.024 | 1.722 | 1.746 | 1.722 | 71.750 | | 8 | 3 | 0.024 | 1.734 | 1.758 | 1.734 | 72.250 | | 8 | 3.5 | 0.024 | 1.745 | 1.769 | 1.745 | 72.708 | | 8 | 4 | 0.024 | 1.756 | 1.781 | 1.756 | 73.167 | | 8 | 4.5 | 0.024 | 1.767 | 1.792 | 1.768 | 73.625 | | 8 | 5 | 0.024 | 1.779 | 1.804 | 1.779 | 74.125 | | 10 | 0 | 0.032 | -0.014 | 0.018 | -0.014 | -0.438 | | 10 | 0.5 | 0.032 | 0.417 | 0.448 | 0.417 | 13.031 | | 10 | 1 | 0.032 | 0.89 | 0.921 | 0.89 | 27.813 | | 10 | 1.5 | 0.032 | 1.367 | 1.398 | 1.367 | 42.719 | | 10 | 2 | 0.032 | 1.838 | 1.867 | 1.838 | 57.438 | | 10 | 2.5 | 0.032 | 2.232 | 2.263 | 2.231 | 69.750 | | 10 | 3 | 0.032 | 2.254 | 2.285 | 2.254 | 70.438 | | 10 | 3.5 | 0.032 | 2.269 | 2.3 | 2.269 | 70.906 | | 10 | 4 | 0.032 | 2.284 | 2.315 | 2.283 | 71.375 | | 10 | 4.5 | 0.032 | 2.299 | 2.329 | 2.298 | 71.844 | | 10 | 5 | 0.032 | 2.313 | 2.344 | 2.313 | 72.281 | | 10 | 5.5 | 0.032 | 2.328 | 2.359 | 2.328 | 72.750 | | 10 | 6 | 0.032 | 2.342 | 2.374 | 2.342 | 73.188 |   Table 1 Multisim calculations    Graph 1 IC vs VCE |

**3.2 Common collector circuit for lab 8**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| Circuit 2 shows the common collector circuit in multisim. I will then show the relationship between gain and frequency in table 2 and graph 2. Section 5 will comment on the results.    Circuit 2 Common Collector Circuit in Multisim   |  |  |  |  | | --- | --- | --- | --- | | Frequency (Hz) | Vin (mV) | Vout (mV) | Gain (dB) | | 10 | 500 | 0.281 | -65.000 | | 30 | 500 | 0.846 | -55.435 | | 60 | 500 | 1.694 | -49.401 | | 100 | 500 | 2.801 | -45.032 | | 200 | 500 | 5.610 | -39.000 | | 500 | 500 | 13.947 | -31.090 | | 1000 | 500 | 28.117 | -25.000 | | 2000 | 500 | 57.302 | -18.816 | | 5000 | 500 | 139.018 | -11.118 | | 10000 | 500 | 281.171 | -5.000 | | 15000 | 500 | 428.519 | -1.340 | | 20000 | 500 | 571.110 | 1.155 | | 50000 | 500 | 1416.022 | 9.042 | | 75000 | 500 | 2120.655 | 12.550 | | 100000 | 500 | 2811.707 | 15.000 | | 150000 | 500 | 4173.208 | 18.430 | | 200000 | 500 | 5465.375 | 20.773 | | 500000 | 500 | 11430.626 | 27.182 | | 750000 | 500 | 14325.837 | 29.143 | | 1000000 | 500 | 16000.001 | 30.103 | | 1500000 | 500 | 17640.870 | 30.951 | | 2000000 | 500 | 18340.873 | 31.289 |   Table 2 VIN, VOUT, Gain according to frequency    Graph 2 Gain vs Frequency |

**~~4. Experimental:~~**

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| We were not instructed to provide experimental results for this lab, see the following screenshot. |

**5. Results and Discussion:**

When analyzing the results from section 3.1, we can see that the results line closely with what we would expect. As we increase our voltages for each series, it takes longer to get to a higher value, which is what we would expect from a BJT. The B value also correlates to this trend. As we get higher in the V1 values, V2 has less immediate effect on B, but it does level out to a higher value. Overall, results are as expected.

For section 3.2, we achieve similar results. We do not necessarily get clipping in multisim, but I would guess it would be around 750Khz as we would begin to outgrow the capacitors at that point. If we wanted to reduce clipping, we would need to introduce larger capacitors into the circuit. If we introduce larger capacitors, our gain will shrink. When looking at the results for lab 8, they are not accurate at all, however. Doing the hand calculations seen in the appendix show very different values from that calculated in multisim. See appendix for details.

Figure 5.1 shows what vout should actually be instead of that calculated in the multisim circuit:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  |  |  | | --- | --- | --- | --- | | Frequency (Hz) | Vin (mV) | Vout (mV) | Gain (dB) | | 10 | 500 | 0.00014059 | -65 | | 30 | 500 | 0.00042285 | -55.435 | | 60 | 500 | 0.00084701 | -49.401 | | 100 | 500 | 0.00140068 | -45.032 | | 200 | 500 | 0.00280505 | -39 | | 500 | 500 | 0.00697333 | -31.09 | | 1000 | 500 | 0.01405853 | -25 | | 2000 | 500 | 0.02865101 | -18.816 | | 5000 | 500 | 0.06950883 | -11.118 | | 10000 | 500 | 0.14058533 | -5 | | 15000 | 500 | 0.21425946 | -1.34 | | 20000 | 500 | 0.28555516 | 1.155 | | 50000 | 500 | 0.70801101 | 9.042 | | 75000 | 500 | 1.06032746 | 12.55 | | 100000 | 500 | 1.40585331 | 15 | | 150000 | 500 | 2.08660387 | 18.43 | | 200000 | 500 | 2.73268774 | 20.773 | | 500000 | 500 | 5.71531286 | 27.182 | | 750000 | 500 | 7.16291848 | 29.143 | | 1000000 | 500 | 8.0000004 | 30.103 | | 1500000 | 500 | 8.8204351 | 30.951 | | 2000000 | 500 | 9.17043651 | 31.289 |   Figure 5.1: Expected vout values for lab 8. |

**6. Conclusion:**

Overall, this lab was very helpful in expanding my knowledge of BJTs, NPN and PNP transistors. Being able to see the values changing in real time as I changed the input voltages showed me how these circuits work. Continually, it gave me the insight into how these circuits can be applied to real world problems. Lastly, doing some quick hand calculations shows that multisim is not always right, and the circuit implemented can give bad results. We can see this in the appendix for lab 8.

**7. Appendix**

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Appendix 1: Hand calculations